HMC361S8G

SMT GaAs HBT MMIC DIVIDE-BY-2, DC - 10.0 GHz

Typical Applications

Prescaler for DC to X Band PLL Applications:

- Satellite Communication Systems
- Fiber Optic
- Pt-Pt and Pt-MPt Radios
- VSAT

Features

Ultra Low SSB Phase Noise: -148 dBc/Hz

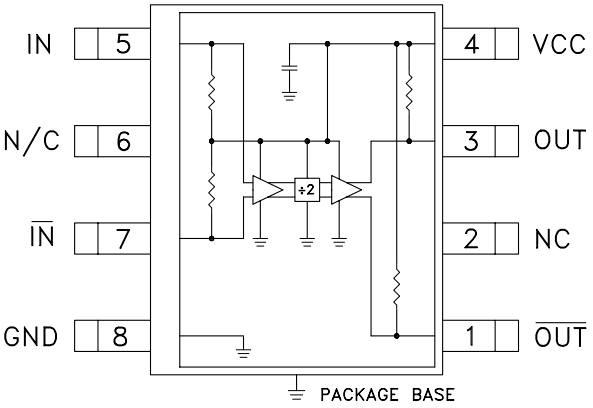
Wide Bandwidth

Output Power: 3 dBm

Single DC Supply: +5V

S8G SMT Package

Functional Diagram



General Description

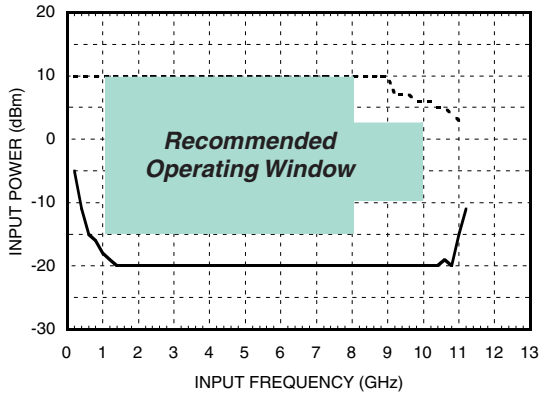
The HMC361S8G is a low noise Divide-by-2 Static Divider with InGaP GaAs HBT technology in an 8 lead surface mount plastic package. This device operates from DC (with a square wave input) to 10 GHz input frequency with a single +5.0V DC supply. The low additive SSB phase noise of -148 dBc/Hz at 100 kHz offset helps the user maintain good system noise performance.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Vcc= 5V

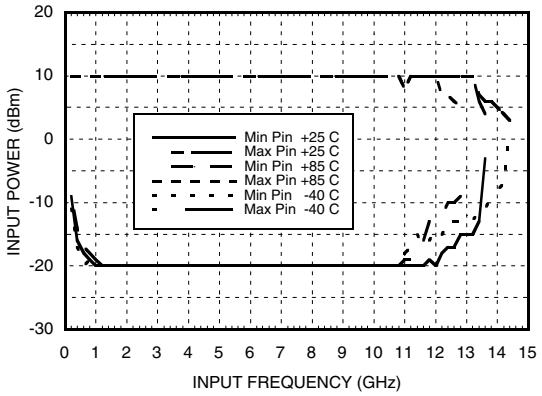
Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency		10	11		GHz
Minimum Input Frequency	Sine Wave Input. [1]		0.2	0.5	GHz
Input Power Range	Fin = 1 to 8 GHz	-15	>-20	+10	dBm
	Fin = 8 to 10 GHz	-10	>-15	+2	dBm
Output Power	Fin = 6 GHz	0	3		dBm
	Fin = 10 GHz	-6			dBm
Reverse Leakage	Both RF Outputs Terminated		45		dB
SSB Phase Noise (100 kHz offset)	Pin = 0 dBm, Fin = 6 GHz		-148		dBc/Hz
Output Transition Time	Pin = 0 dBm, Fout = 882 MHz		100		ps
Supply Current (Icc)			83		mA

1. Divider will operate down to DC for square-wave input signal.

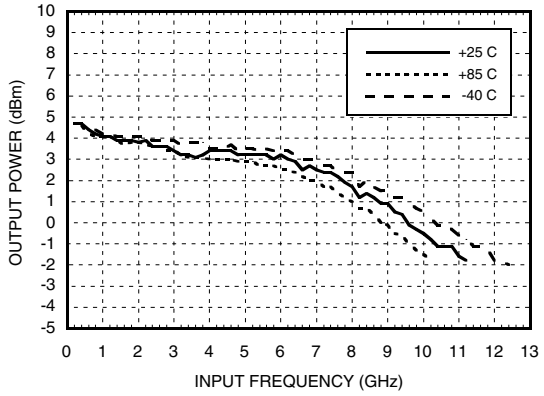
Input Sensitivity Window, T= 25 °C



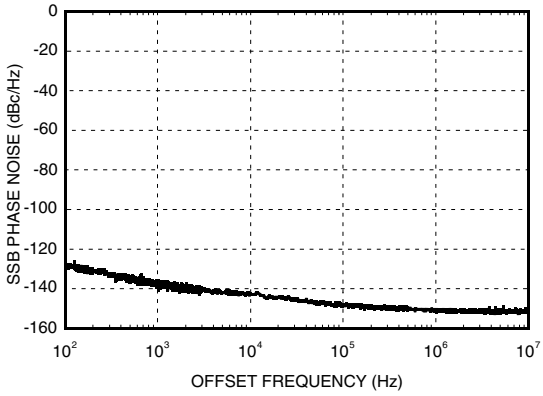
Input Sensitivity Window vs. Temperature



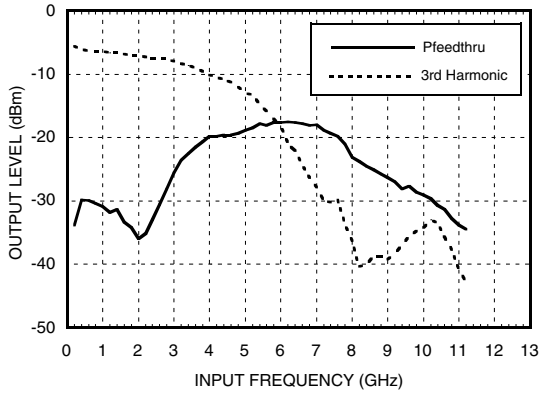
Output Power vs. Temperature



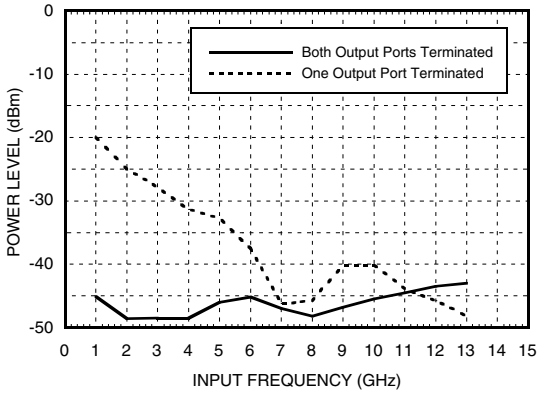
SSB Phase Noise Performance, Pin= 0 dBm, T= 25 °C



Output Harmonic Content, Pin= 0 dBm, T= 25 °C



Reverse Leakage, Pin= 0 dBm, T= 25 °C



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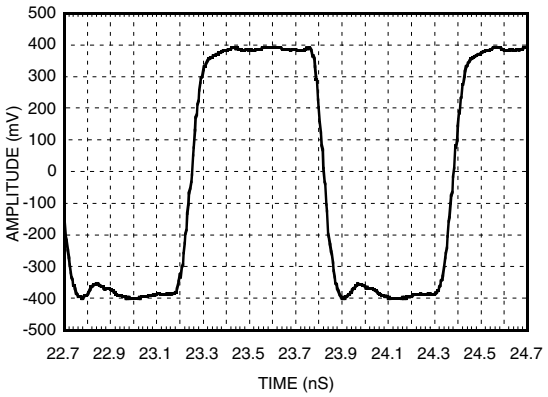
Output Voltage Waveform, Pin= 0 dBm, Fout= 882 MHz, T= 25 °C



Absolute Maximum Ratings

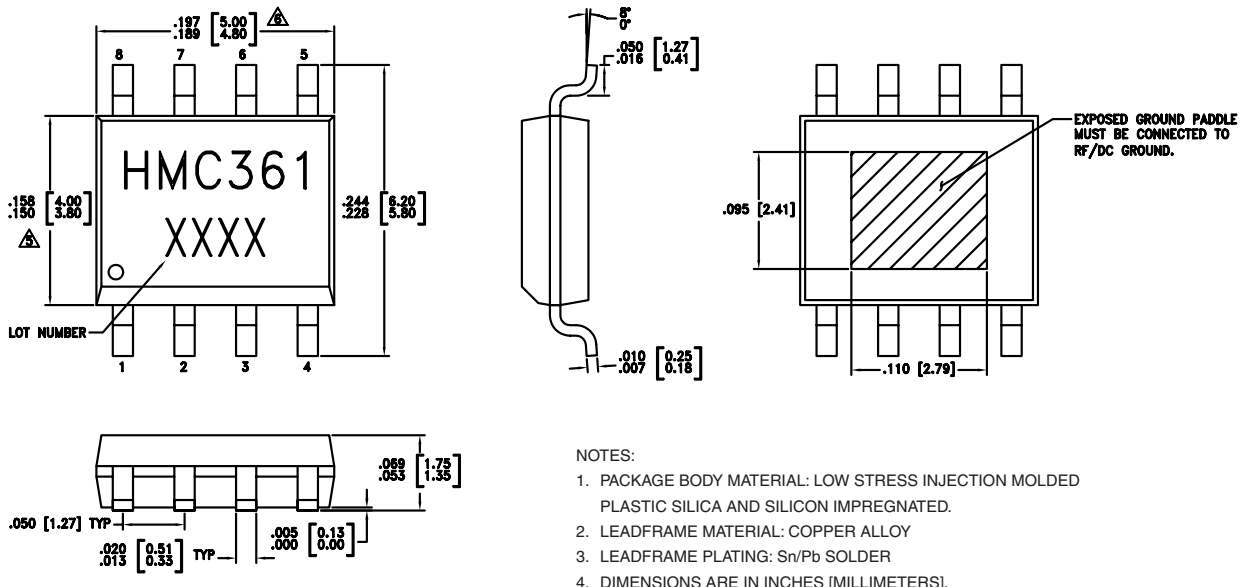
RF Input (Vcc = +5V)	+13 dBm
Vcc	+5.5V
VLogic	Vcc -1.6V to Vcc -1.2V
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
4.75	74
5.0	83
5.25	89

Note: Divider will operate over full voltage range shown above

Outline Drawing

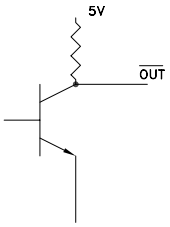
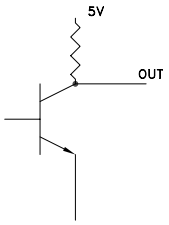
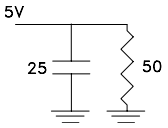
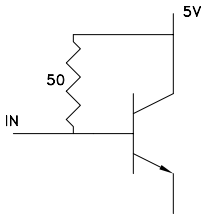
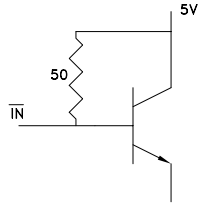


NOTES:

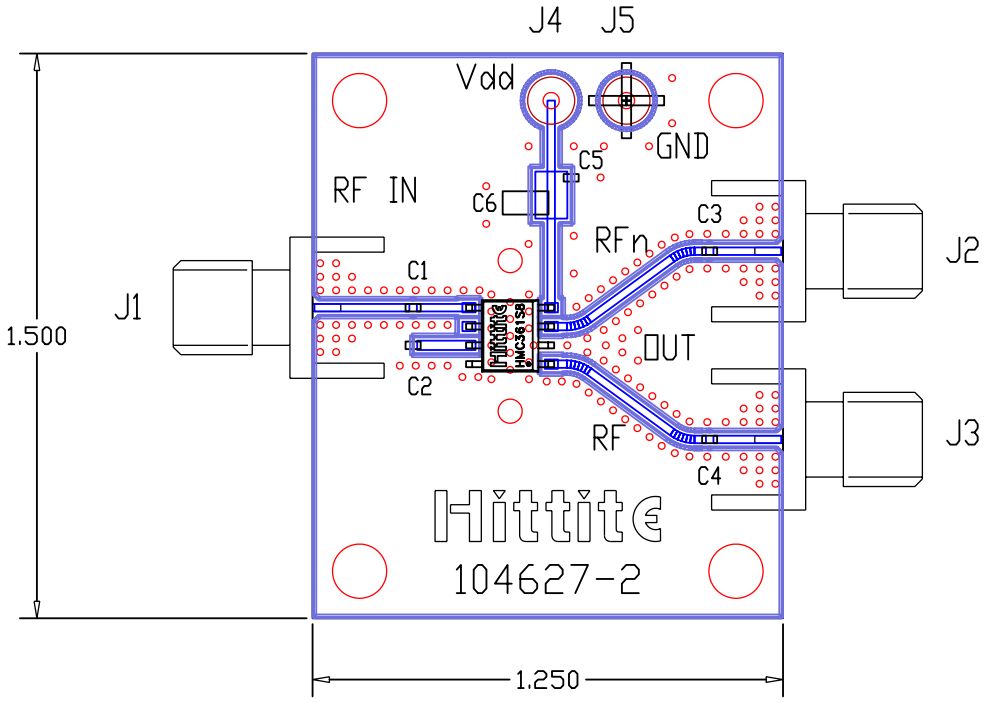
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEADFRAME MATERIAL: COPPER ALLOY
3. LEADFRAME PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
12 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order Online at www.hittite.com

Pin Description

Pin Number	Function	Description	Interface Schematic
1	$\overline{OUT}$	Divided output 180° out of phase with pin 3.	
2, 6	N/C	No connection. These pins must not be grounded.	
3	OUT	Divided Output.	
4	VCC	Supply voltage 5V ± 0.25V.	
5	IN	RF Input must be DC blocked.	
7	$\overline{IN}$	RF Input 180° out of phase with pin 5 for differential operation. A/C ground for single ended operation	
8	GND	Ground Backside of package has exposed metal ground slug which must be connected to ground.	

Evaluation PCB



List of Materials

Item	Description
J1 - J3	PC Mount SMA RF Connector
C1 - C4	100 pF Capacitor, 0402 Pkg.
C5	1000 pF Capacitor, 0603 Pkg.
C6	10 µF Tantalum Capacitor
U1	HMC361S8G Divide-by-2
PCB*	104627 Eval Board
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. This evaluation board is designed for single ended input testing. J2 and J3 provide differential output signals.

Application Circuit